ABSTRACT OF THE DISCLOSURE

The synchronization signal generating section generates a packet synchronization signal PSYNC such that it is synchronized with the cycle of packets received from the master device. The interface control section generates a transfer clock PCMCLK used in transferring the data in the packets, from the internal clock. The interface control section measures the cycle of the packet synchronization signal PSYNC, and if the actual cycle of PSYNC is longer than the designated value, it makes the cycle of the transfer clock corresponding to the last data element in the packet longer than the cycle of the transfer clock corresponding to the other data elements, whereas if the actual cycle of PSYNC is shorter than the designated value, it makes the cycle of the transfer clock corresponding to the last data element in the packet shorter than the cycle of the transfer clock corresponding to the other data elements.